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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,591	02/06/2004	Jose P. Pereira	P249-2/WLP	8956

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EXAMINER	
PEIKARI, BEHZAD	

ART UNIT	PAPER NUMBER
2189	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,591	PEREIRA, JOSE P.	
	Examiner	Art Unit	
	B. James Peikari	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 24-41* is/are rejected.

7)☒ Claim(s) *22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4-21, 24-34, 36 and-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Nataraj (US Pub No 2002/0129198).

As per claims 1 and 36, Nataraj discloses a content addressable memory (CAM) device for comparing a search key to data values stored therein (Paragraph 354, Lines 5-12), comprising:

a plurality of CAM blocks, each CAM block including an array of CAM cells divided into a plurality of segments (Fig 60, Ref 6001), each array segment for storing a number of data values that are assigned the same priority (Fig 56, Ref 5603); and

a plurality of block priority circuits (Fig 60, Ref 6003, 6005, 6007), each having inputs to receive match signals from a corresponding CAM block (Fig 60, Ref 6005) , outputs to generate a block index (Fig 56, Ref 5601; Fig 60 "RIN") and the priority of a matching data value (Fig 56, Ref 5603; Fig 60, "BPN"), and an address table for storing address information for each array segment in the corresponding CAM block [Priority index table (Paragraph 361)].

As per claim 24, Nataraj discloses a content addressable memory (CAM) device having plurality of CAM blocks, each comprising:

an array of CAM cells divided into a plurality of segments (Fig 60, Ref 6001), each array segment for storing a number of data values that are assigned the same priority (Fig 56, Ref 5603);

means for generating a row index of a highest priority matching value (Fig 56, Ref 5601, 5603; Fig 60 "RIN"; Fig 60 "BPN");

means for storing address information for each array segment (Fig 60, Ref 6011); and

means for comparing the row index with the address information to determine which priority the highest priority matching data value is assigned (Fig 59, Ref 5905).

As per claims 2 and 25, Nataraj discloses the CAM device of Claim 1 wherein each CAM block is assigned to store a predetermined content range of data values (Paragraph 96, Lines 12-13).

As per claims 4 and 26, Nataraj discloses the CAM device of Claim 2, further comprising:

means for extracting a selected portion of the search key in response to a select signal [Nataraj discloses selecting a comparand word size (Paragraph 225, Lines 1-4)]; and

means for selectively enabling each CAM block in response to a comparison between the selected portion of the search key and the predetermined range of data values for the corresponding CAM block (Paragraph 355).

As per claims 5 and 27, Nataraj discloses the CAM device of Claim 1, wherein the address information comprises a start address for each array segment [Table stores all addresses thus there must be a start address for each array segment (Paragraph 361)].

As per claim 6 and 28, Nataraj discloses the CAM device of Claim 1, wherein the address information comprises an address range for each array segment [Table stores all addresses thus there must be an address range for each array segment (Paragraph 361)].

As per claim 7, Nataraj discloses the CAM device of Claim 1, wherein each block priority circuit compares the block index with the address information to determine the priority assigned to the matching data value (Paragraph 361, Lines 6-13).

As per claim 8, Nataraj discloses the CAM device of Claim 1, wherein each block priority circuit further comprises:

a priority encoder having inputs to receive the match signals from the corresponding CAM block and having an output to generate a row index the matching data value (Fig 60, Ref 6005; Paragraph 344, Lines 10-12);

a compare circuit having first inputs to receive the address information, second input to receive the row index, and a plurality of outputs (Paragraph 344, Lines 5-10); and

a priority table having a plurality of rows, each for storing the priority assigned to a corresponding array segment and having an input coupled to a corresponding output of the compare circuit, the priority table having an output to generate the priority of the matching data value (Fig 60, Ref 6003).

As per claim 9, Nataraj discloses the CAM device of Claim 8, wherein the compare circuit compares the row index with the address information to selectively enable one of the rows of the priority table (Paragraph 344, Lines 14-19).

As per claim 10, Nataraj discloses the CAM device of Claim 9, wherein the compare circuit asserts one of a plurality of priority select signals in response to the comparison between the row index and the address information (Paragraph 344, Lines 5-10).

As per claim 11, Nataraj discloses the CAM device of Claim 8, wherein each block priority circuit further comprises:

a memory to store a block identification (ID) for the corresponding CAM block (Paragraph 377); and

means for concatenating the block ID to the row index to generate the block index (Paragraph 377).

As per claim 12, Nataraj discloses the CAM device of Claim 1, further comprising:

a global priority and index circuit having inputs to receive the block indexes and priorities from the block priority circuits, and having an output to generate a device index of the highest priority matching data value (Paragraph 372, Lines 3-8).

As per claim 13, Nataraj discloses the CAM device of Claim 12, wherein the global priority and index circuit comprises:

compare logic having inputs to receive the priorities from the block priority circuits and having outputs to generate select signals for corresponding CAM blocks (Fig 60, Ref 6033; Fig 65, Ref 6501); and

a select circuit having first inputs to receive the block indexes, second inputs to receive the select signals, and an output to generate the device index (Fig 60, Ref 6033; Fig 65, Ref 6503).

As per claim 14, Nataraj discloses the CAM device of Claim 13, wherein the select circuit selectively outputs one of the block indexes as the device index in response to the select signals (Paragraph 411, Lines 1-7).

As per claim 15, Nataraj discloses the CAM device of Claim 13, wherein the compare logic compares the priorities with each other to determine which priority is the highest (Paragraph 381).

As per claim 16, Nataraj discloses the CAM device of Claim 15, wherein the compare logic includes a second output to generate the highest priority [Note compare logic outputs second lines to priority encoder to generate highest priority (Fig 65, Ref 6505)].

As per claim 17, Nataraj discloses the CAM device of Claim 1, wherein each block priority circuit comprises:

a priority encoder and match flag circuit having a plurality of segments, each segment including inputs to receive the match signals from a corresponding array segment and having outputs to generate a row index and a segment match flag for the corresponding array segment (Fig 60, Ref 6007); and

a priority circuit having inputs to receive the row indexes and segment match flags and having outputs to generate a device index and priority of a highest priority matching data value (Fig 60, Ref 6005).

As per claim 18, the CAM device of Claim 17, wherein the priority circuit is configured to re-order the row indexes and match flags according to priority [Nataraj discloses ordering the blocks according to priority, thus disclosing reordering (Paragraph 100)].

As per claim 19, Nataraj discloses the CAM device of Claim 17, wherein the priority circuit further comprises:

means for storing the priority assigned to each array segment (Fig 4, Ref 408; Fig 59, Ref 5605).

As per claim 20, Nataraj discloses the CAM device of Claim 17, wherein the priority circuit further comprises:

a priority table having a plurality of rows each for storing the priority assigned to a corresponding array segment (Fig 60, Ref 6003);

compare logic having a plurality of inputs to receive the priorities from the priority table and having an output (Paragraph 344, Lines 5-10);

first multiplexer having a plurality of inputs to receive the priorities from the priority table, an output to generate a block priority, and a control terminal coupled to the output the compare logic (Fig 59, Ref 5905); and

a second multiplexer having a plurality of inputs each to receive the row index from a corresponding array segment, a control terminal coupled to the output of the

compare logic, and an output to selectively output one of the row indexes (Fig 59, Ref 5605).

As per claim 21, Nataraj discloses the CAM device of Claim 19, wherein each row of the priority table is responsive to a corresponding segment match flag (Fig 15, Ref 1503 , 1507).

As per claim 29, Nataraj discloses the CAM device of Claim 24, wherein the means for and the means for generating and the means for comparing comprises a priority circuit (Fig 59).

As per claim 30, Nataraj discloses the CAM device of Claim 29, wherein the priority circuit comprises an address table having a plurality of rows, each for storing address information for a corresponding array segment block [Priority index table (Paragraph 361)].

As per claim 31, Nataraj discloses the CAM device of Claim 29, wherein the means for comparing comprises a compare circuit having first inputs receive the address information from the address table, a second input to receive the row index, and outputs to generate a priority select signal for each array segment (Paragraph 344, Lines 5-10).

As per claim 32, Nataraj discloses the CAM device of Claim 31, wherein each CAM block further comprises:

a priority table having a plurality of rows, each for storing the priority assigned to a corresponding array segment and each responsive to a corresponding priority select signal (Fig 60, Ref 6003).

As per claim 33, Nataraj discloses the CAM device of Claim 32, wherein each CAM block further comprises:

means for storing the priorities assigned to each of the array segments (Fig 4, Ref 408; Fig 59, Ref 5605)

As per claim 34, Nataraj discloses the CAM device of Claim 24 wherein each CAM block further comprises:

Means for re-ordering the priorities of the array segments [Nataraj discloses ordering the blocks according to priority, thus disclosing reordering (Paragraph 100)].

As per claim 40, Nataraj discloses a method of operating a content addressable memory (CAM) device having an array of CAM cells divided into a plurality of array segments, comprising:

assigning a different priority to each of the array segments (Fig 56, Ref 5603);

storing address information for each array segment [Priority index table (Paragraph 361)];

generating a segment match flag and a row index of a matching data value stored each array segment (Fig 56, Ref 5601 and 5603); and

comparing the row indexes with the address information to determine the priorities of the matching data values (Fig 59, Ref 5905).

As per claim 41, Nataraj discloses the method of Claim 40, further comprising:

re-ordering the row indexes and segment match flags according to their assigned priorities [Nataraj discloses ordering the blocks according to priority, thus disclosing reordering (Paragraph 100)].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nataraj as applied to claim 2 above, and further in view of Sherman (US Patent 6,389,507).

As per claim 3, Nataraj discloses the CAM device of Claim 2. Nataraj does not disclose the CAM device further comprising an overflow CAM block that can store any

data value, regardless of content. Sherman discloses such an overflow CAM block (Col 13, Lines 3-6)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the overflow CAM block of Sherman into the system of Nataraj, since Nataraj and Sherman form the same field of endeavor, namely CAM storage and this would allow for storage of overflow entries (Col 13, Lines 7-9).

5. Claims 35 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nataraj as applied to claim 34 above, and further in view of Stormon (US Patent 5,649,149)

As per claim 35, Nataraj discloses the CAM device of Claim 34. Nataraj does not disclose the CAM device wherein the means for re-ordering comprises a plurality of re-order registers, each for storing a re-order value. Stormon discloses such a device wherein the means for re-ordering comprises a plurality of re-order registers, each for storing a re-order value (Col 6, Lines 27-35).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the reprioritization of Stormon into the system of Nataraj, since Nataraj and Stormon form the same field of endeavor, namely CAM storage and this would allow for proper selection of the CAM word for access (Col 6, Line 35).

As per claim 37, Nataraj discloses the method of Claim 35, wherein the address information comprises a start address for each array segment [Table stores all addresses thus there must be a start address for each array segment (Paragraph 361)].

As per claim 38, Nataraj discloses the method of Claim 35, wherein the address information comprises an address range for each array segment [Table stores all addresses thus there must be an address range for each array segment (Paragraph 361)].

As per claim 39, Nataraj discloses the method of Claim 35, further comprising:

storing the priorities assigned to the array segments in a priority table (Fig 60, Ref 6003).

Allowable Subject Matter

6. Claims 22 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed on August 21, 2006 have been fully considered but they are not persuasive.

(A) With regard to applicant's statements throughout the remarks that "Nataraj's priority index table does not store address information for each array segment in the corresponding CAM block", this is not correct.

Applicant further states that "priority index table 6003 in Nataraj stores a priority number for each of the rows in Nataraj's CAM array to indicate the priorities of data stored in the array"; this is only partially correct.

As stated in paragraph [0361], the index table 6003, together with the encoder 6005, generates, for each corresponding block, "a highest priority number *and corresponding match address*" (emphasis added).

Clearly, information in the table 6003 used to generate an address *is* "address information", as claimed. Nataraj also calls this address a block index number (BIN). See Figure 60.

Furthermore, it is noted that each block is a segment of the memory array, as claimed.

(B) With regard to applicant's statement on page 13 of the remarks that "Nataraj's MUX 5905 does not compare the row address with the address information", suggesting that the "selection" made by the MUX does not involve a comparator, this is not correct.

In data processing systems, true "selection" is made either by random selection or by comparison. When random selection is used, a random number generator is required. When comparison is used, a comparator or MUX (usually having at least one XOR gate inside) is required.

Nataraj's row priority encoder circuitry utilizes select logic 5607, which has a MUX 5905 and no random number generator. Clearly, the MUX 5905 is for comparison. See Figures 58 and 59.

(C) With regard to the dependent claims 2-21, 25-35, 37-39 and 41, applicant's remarks indicate that they should be allowable because the independent claims are allowable. Since applicant has not rebutted any of the rejections directed to the particular features of these claims, these claims are deemed to stand or fall with the independent claims. Consequently, the present examiner has maintained these rejections as presented in the previous Office action.

Conclusion

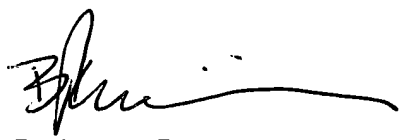
8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (571) 272-4185. The examiner is generally available between 7:00 am and 7:30 pm, EST, Monday through Wednesday, and between 5:30 am and 4:00 pm on Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon, can be reached at (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center at 866-217-9197 (toll-free).



B. James Peikari
Primary Examiner
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11/11/06